Amendments to the Specification:

Please amend the following paragraph beginning at page 2, line 15 as follows:

The DLL circuit according to the second conventional technique comprises: a duty cycle correction amplifier 700 which corrects the duty cycle of an input reference clock signal and outputs a duty cycle corrected signal; a phase detector 710 which compares the phase of a clock signal output from the DLL circuit with the phase of a reference clock signal and generates and outputs a signal which indicates whether the phase of the output clock signal is in advance of or delays from the phase of the reference clock signal; a charge pump 720 (preferably a differential charge pump) which is driven by a signal output from the phase detector ~~700~~ 710 and generates an output current according to the output signal: a phase shifter 730 into which the duty cycle corrected signal, a signal output from the phase detector 710, and a current output from the charge pump 720 are input and which performs phase shifting of the duty cycle corrected signal to a direction indicated by the signal output from the phase detector 710 and outputs a phase s corrected signal; a second duty, cycle corrector 740 into which the phase corrected signal output from the phase shifter 730 and an output clock signal are input to correct the duty cycle of the output clock signal to a desired value; and a buffer amplifier 750 for amplifying the output clock signal to a predetermined amplitude.

Please amend the following paragraphs beginning at page 9, line 8 as follows:

The invention will be explained in more detail in conjunction with the appended drawings. ~~, wherein:~~

Fig. 1 is a block diagram showing the construction of a DLL circuit according to a first conventional ~~technique;~~ technique.

Fig, 2 is a block diagram showing the construction of a DLL circuit according to a second conventional ~~technique;~~ technique.

Fig. 3 is a circuit diagram of a phase detector as one major element in the DLL circuit according to the second conventional ~~technique;~~ technique.

Fig. 4 is a circuit diagram of a duty cycle correction amplifier as another major element in the DLL circuit according to the second conventional ~~technique;~~ technique.

Fig. 5 is a block diagram of a phase shifter as a further element in the DLL circuit according to the second conventional ~~technique;~~ technique.

Fig. 6 is a block diagram showing a phase interpolator included in the phase shifter shown in ~~Fig. 5;~~ Fig. 5.

Please amend the following paragraphs beginning at page 10, line 8 as follows:

Fig. 11 is a diagram illustrating a counting circuit and correction signal generation means, wherein Fig. 11A is a schematic block diagram of the counting circuit and the correction signal generation means and Fig. 11B a graph showing an example of the relationship between the results of counting by the counting circuit and the value of current which flows through PMOS in a second bias generation ~~circuit;~~ circuit.

Fig. ~~11~~ 12 is a block diagram showing a DLL circuit according to a second preferred embodiment of the ~~invention;~~ invention.

Fig. ~~12~~ 13 is a typical circuit diagram of one functional block in its final stage portion included in the DLL circuit according to the ~~invention; and~~ invention.

Fig. 14 is a typical timing chart for major signals associated with counting control means.

Please amend the following paragraph beginning at page 10, line 26 as follows:

Fig. 7 is a diagram illustrating a DLL circuit according to a first preferred embodiment of the invention. ~~wherein Fig. 8A is a schematic block diagram showing the construction of a DLL circuit 100 and Fig. 8B a schematic block diagram showing the construction of bias generation means 200 included in this DLL circuit 100.~~

Please amend the following paragraph beginning at page 11, line 27 as follows:

~~The~~ With reference to Fig. 8, bias generation means 200 comprises: a first bias generation circuit 250 which generates a primary bias signal 392 such that, when the frequency of the signal 300 input into the DLL circuit 100 is the highest, the current value of a constant-current source in each differential amplifier circuit is brought to a predetermined current value Is1 at which each differential amplifier circuit is normally operated; bias control means 210 which outputs a bias correction signal 380 for

correcting the primary bias signal 392 according to the frequency of the input signal 300; and a second bias generation circuit 270 which, based on the primary bias signal 392 and the -.bias correction signal 380, generates an internal bias signal 395 such that the current value of the constant-current source is brought to a value which enables each differential amplifier circuit to be operated at the frequency of the input signal 300.

Please amend the ABSTRACT as follows:

~~Disclosed is a~~ A DLL (delay locked loop) circuit for outputting a phase lock signal having a predetermined phase relationship with an input signal. The DLL circuit has: a functional block having a constant-current source; and bias ~~generation means~~ generator for generating a constant current source bias signal for controlling the constant current source of the functional block, the bias ~~generation means~~ generator comprising a bias control ~~means~~ which changes the bias signal according to the frequency of the input signal.